Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A process for producing a mask layer for a semiconductor substrate, the process which comprises:

providing a configuration including a semiconductor substrate, a first layer configuration configured on the semiconductor substrate, a second layer configured on the first layer configuration, and a third layer configured on the second layer, the first layer configuration being a ferroelectric or dielectric layer configuration of a plurality of individual layers including an upper layer having a metal, a middle layer having barium-strontium-titanate ~~or strontium-bismuth-tantalate~~, and a lower layer having iridium or iridium oxide;

patterning the third layer to form a first trench, which uncovers the second layer, in the third layer;

using the third layer as an etching mask, etching the second layer and forming a second trench in the second layer near the

first trench, the second trench uncovering the upper layer of the first layer configuration;

removing the third layer from the second layer;

using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer configuration and forming a third trench in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate;

after forming the third trench, depositing a fourth layer of an insulating material on the semiconductor substrate;

chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place in the third trench.

Claim 2 (original). The process according to claim 1, wherein the upper layer of the first layer arrangement includes tungsten, tantalum, titanium, copper, titanium nitride, tantalum nitride, tungsten silicide, tungsten nitride,

platinum, iridium, cobalt, palladium, silicide, nitride, or carbide.

Claim 3 (original). The process according to claim 1, wherein the third layer is a photosensitive mask layer.

Claim 4 (original). The process according to claim 1, wherein the fourth layer includes silicon oxide, silicon nitride, butylcyclobutene, or polybutyl oxalate.

Claim 5 (original). The process according to claim 1, which further comprises performing the chemically mechanically polishing step using a polishing fluid having a solids content of between 20% and 40%.

Claim 6 (original). The process according to claim 1, which further comprises performing the chemically mechanically polishing step using a polishing fluid including ammonia.

Claim 7 (original). The process according to claim 1, which further comprises performing the chemically mechanically polishing step using a polishing fluid having a pH between 9 and 11.

Claim 8 (withdrawn). A process for producing a mask layer for a semiconductor substrate, the process which comprises:

providing a configuration including a semiconductor substrate, a first layer configuration configured on the semiconductor substrate, a second layer configured on the first layer configuration, and a third layer configured on the second layer, the first layer configuration being a magneto-resistive layer configuration of a plurality of individual layers including an upper layer having a metal, a middle layer, and a lower layer having aluminum oxide, aluminum nitride or titanium oxide;

patterning the third layer to form a first trench, which uncovers the second layer, in the third layer;

using the third layer as an etching mask, etching the second layer and forming a second trench in the second layer near the first trench, the second trench uncovering the upper layer of the first layer configuration;

removing the third layer from the second layer;

using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer

configuration and forming a third trench in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate;

after forming the third trench, depositing a fourth layer of an insulating material on the semiconductor substrate;

chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place in the third trench.

Claim 9 (withdrawn). The process according to claim 8, wherein the upper layer of the first layer arrangement includes tungsten, tantalum, titanium, copper, titanium nitride, tantalum nitride, tungsten silicide, tungsten nitride, platinum, iridium, cobalt, palladium, silicide, nitride, or carbide.

Claim 10 (withdrawn). The process according to claim 8, wherein the third layer is a photosensitive mask layer.

Claim 11 (withdrawn). The process according to claim 8, wherein the fourth layer includes silicon oxide, silicon nitride, butylcyclobutene, or polybutyl oxalate.

Claim 12 (withdrawn). The process according to claim 8, which further comprises performing the chemically mechanically polishing step using a polishing fluid having a solids content of between 20% and 40%.

Claim 13 (withdrawn). The process according to claim 8, which further comprises performing the chemically mechanically polishing step using a polishing fluid including ammonia.

Claim 14 (withdrawn). The process according to claim 8, which further comprises performing the chemically mechanically polishing step using a polishing fluid having a pH between 9 and 11.

Claim 15 (new). A process for producing a mask layer for a semiconductor substrate, the process which comprises:

providing a configuration including a semiconductor substrate, a first layer configuration configured on the semiconductor substrate, a second layer configured on the first layer configuration, and a third layer configured on the second

layer, the first layer configuration being a ferroelectric or dielectric layer configuration of a plurality of individual layers including an upper layer having a metal, a middle layer having strontium-bismuth-tantalate, and a lower layer having iridium or iridium oxide;

patterning the third layer to form a first trench in the third layer, uncovering the second layer,;

using the third layer as an etching mask, etching the second layer and forming a second trench in the second layer near the first trench, the second trench uncovering the upper layer of the first layer configuration;

removing the third layer from the second layer;

using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer configuration and forming a third trench in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate;

after forming the third trench, depositing a fourth layer of an insulating material on the semiconductor substrate;

chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place in the third trench.